

HWV axioms

HWV001-0.ax Connections, faults, and gates.

$(\text{connection}(p_1, p_2) \text{ and } \text{value}(p_1, v)) \Rightarrow \text{value}(p_2, v)$ $\text{cnf}(\text{value_propagation}_1, \text{axiom})$
 $(\text{connection}(p_1, p_2) \text{ and } \text{value}(p_2, v)) \Rightarrow \text{value}(p_1, v)$ $\text{cnf}(\text{value_propagation}_2, \text{axiom})$
 $(\text{value}(p, v_1) \text{ and } \text{value}(p, v_2)) \Rightarrow \text{equal_value}(v_1, v_2)$ $\text{cnf}(\text{unique_value}, \text{axiom})$
 $\neg \text{equal_value}(n_0, n_1)$ $\text{cnf}(\text{equal_value}_1, \text{axiom})$
 $\neg \text{equal_value}(n_1, n_0)$ $\text{cnf}(\text{equal_value}_2, \text{axiom})$
 $\text{mode}(k, \text{ok}) \Rightarrow \neg \text{mode}(k, \text{abnormal})$ $\text{cnf}(\text{not_ok_and_abnormal}, \text{axiom})$
 $\text{type}(k, \text{any}) \Rightarrow (\text{mode}(k, \text{ok}) \text{ or } \text{mode}(k, \text{abnormal}))$ $\text{cnf}(\text{ok_or_abnormal}, \text{axiom})$
 $(\text{mode}(k, \text{ok}) \text{ and } \text{type}(k, \text{and}) \text{ and } \text{value}(\text{in}(\text{any}, k), n_0)) \Rightarrow \text{value}(\text{out}(n_1, k), n_0)$ $\text{cnf}(\text{and_0x}_0, \text{axiom})$
 $(\text{mode}(k, \text{ok}) \text{ and } \text{type}(k, \text{and}) \text{ and } \text{value}(\text{in}(n_1, k), n_1) \text{ and } \text{value}(\text{in}(n_2, k), n_1)) \Rightarrow \text{value}(\text{out}(n_1, k), n_1)$ $\text{cnf}(\text{and_11}_1, \text{axiom})$
 $(\text{mode}(k, \text{ok}) \text{ and } \text{type}(k, \text{and}) \text{ and } \text{value}(\text{out}(n_1, k), n_0)) \Rightarrow (\text{value}(\text{in}(n_1, k), n_0) \text{ or } \text{value}(\text{in}(n_2, k), n_0))$ $\text{cnf}(\text{and_00}_0, \text{axiom})$
 $(\text{mode}(k, \text{ok}) \text{ and } \text{type}(k, \text{and}) \text{ and } \text{value}(\text{out}(n_1, k), n_1)) \Rightarrow \text{value}(\text{in}(n_1, k), n_1)$ $\text{cnf}(\text{and_1_1x}, \text{axiom})$
 $(\text{mode}(k, \text{ok}) \text{ and } \text{type}(k, \text{and}) \text{ and } \text{value}(\text{out}(n_1, k), n_1)) \Rightarrow \text{value}(\text{in}(n_2, k), n_1)$ $\text{cnf}(\text{and_1_x}_1, \text{axiom})$
 $(\text{mode}(k, \text{ok}) \text{ and } \text{type}(k, \text{or}) \text{ and } \text{value}(\text{in}(\text{any}, k), n_1)) \Rightarrow \text{value}(\text{out}(n_1, k), n_1)$ $\text{cnf}(\text{or_1x}_1, \text{axiom})$
 $(\text{mode}(k, \text{ok}) \text{ and } \text{type}(k, \text{or}) \text{ and } \text{value}(\text{in}(n_1, k), n_0) \text{ and } \text{value}(\text{in}(n_2, k), n_0)) \Rightarrow \text{value}(\text{out}(n_1, k), n_0)$ $\text{cnf}(\text{or_00}_0, \text{axiom})$
 $(\text{mode}(k, \text{ok}) \text{ and } \text{type}(k, \text{or}) \text{ and } \text{value}(\text{out}(n_1, k), n_1)) \Rightarrow (\text{value}(\text{in}(n_1, k), n_1) \text{ or } \text{value}(\text{in}(n_2, k), n_1))$ $\text{cnf}(\text{or_11}_1, \text{axiom})$
 $(\text{mode}(k, \text{ok}) \text{ and } \text{type}(k, \text{or}) \text{ and } \text{value}(\text{out}(n_1, k), n_0)) \Rightarrow \text{value}(\text{in}(n_1, k), n_0)$ $\text{cnf}(\text{or_0_0x}, \text{axiom})$
 $(\text{mode}(k, \text{ok}) \text{ and } \text{type}(k, \text{or}) \text{ and } \text{value}(\text{out}(n_1, k), n_0)) \Rightarrow \text{value}(\text{in}(n_2, k), n_0)$ $\text{cnf}(\text{or_0}_01, \text{axiom})$
 $(\text{mode}(k, \text{ok}) \text{ and } \text{type}(k, \text{not}) \text{ and } \text{value}(\text{in}(n_1, k), n_0)) \Rightarrow \text{value}(\text{out}(n_1, k), n_1)$ $\text{cnf}(\text{not_0_1_fw}, \text{axiom})$
 $(\text{mode}(k, \text{ok}) \text{ and } \text{type}(k, \text{not}) \text{ and } \text{value}(\text{in}(n_1, k), n_1)) \Rightarrow \text{value}(\text{out}(n_1, k), n_0)$ $\text{cnf}(\text{not_1_0_fw}, \text{axiom})$
 $(\text{mode}(k, \text{ok}) \text{ and } \text{type}(k, \text{not}) \text{ and } \text{value}(\text{out}(n_1, k), n_0)) \Rightarrow \text{value}(\text{in}(n_1, k), n_1)$ $\text{cnf}(\text{not_0_1_bw}, \text{axiom})$
 $(\text{mode}(k, \text{ok}) \text{ and } \text{type}(k, \text{not}) \text{ and } \text{value}(\text{out}(n_1, k), n_1)) \Rightarrow \text{value}(\text{in}(n_1, k), n_0)$ $\text{cnf}(\text{not_1_0_bw}, \text{axiom})$

HWV001-1.ax Half-adder.

$\text{type}(x, \text{halfadder}) \Rightarrow \text{type}(\text{and}_1(x), \text{and})$ $\text{cnf}(\text{halfadder_and}_1, \text{axiom})$
 $\text{type}(x, \text{halfadder}) \Rightarrow \text{type}(\text{and}_2(x), \text{and})$ $\text{cnf}(\text{halfadder_and}_2, \text{axiom})$
 $\text{type}(x, \text{halfadder}) \Rightarrow \text{type}(\text{not}_1(x), \text{not})$ $\text{cnf}(\text{halfadder_not}_1, \text{axiom})$
 $\text{type}(x, \text{halfadder}) \Rightarrow \text{type}(\text{or}_1(x), \text{or})$ $\text{cnf}(\text{halfadder_or}_1, \text{axiom})$
 $\text{type}(x, \text{halfadder}) \Rightarrow \text{connection}(\text{in}(n_1, x), \text{in}(n_1, \text{or}_1(x)))$ $\text{cnf}(\text{halfadder_connection_in1_in1or}_1, \text{axiom})$
 $\text{type}(x, \text{halfadder}) \Rightarrow \text{connection}(\text{in}(n_2, x), \text{in}(n_2, \text{or}_1(x)))$ $\text{cnf}(\text{halfadder_connection_in2_in2or}_1, \text{axiom})$
 $\text{type}(x, \text{halfadder}) \Rightarrow \text{connection}(\text{in}(n_1, x), \text{in}(n_1, \text{and}_2(x)))$ $\text{cnf}(\text{halfadder_connection_in1_in1and}_2, \text{axiom})$
 $\text{type}(x, \text{halfadder}) \Rightarrow \text{connection}(\text{in}(n_2, x), \text{in}(n_2, \text{and}_2(x)))$ $\text{cnf}(\text{halfadder_connection_in2_in2and}_2, \text{axiom})$
 $\text{type}(x, \text{halfadder}) \Rightarrow \text{connection}(\text{out}(s, x), \text{out}(n_1, \text{and}_1(x)))$ $\text{cnf}(\text{halfadder_connection_outs_out1and}_1, \text{axiom})$
 $\text{type}(x, \text{halfadder}) \Rightarrow \text{connection}(\text{out}(c, x), \text{out}(n_1, \text{and}_2(x)))$ $\text{cnf}(\text{halfadder_connection_outc_out1and}_2, \text{axiom})$
 $\text{type}(x, \text{halfadder}) \Rightarrow \text{connection}(\text{out}(n_1, \text{or}_1(x)), \text{in}(n_1, \text{and}_1(x)))$ $\text{cnf}(\text{halfadder_connection_out1or}_1_in1_and}_1, \text{axiom})$
 $\text{type}(x, \text{halfadder}) \Rightarrow \text{connection}(\text{out}(n_1, \text{and}_2(x)), \text{in}(n_1, \text{not}_1(x)))$ $\text{cnf}(\text{halfadder_connection_out1and}_2_in1not}_1, \text{axiom})$
 $\text{type}(x, \text{halfadder}) \Rightarrow \text{connection}(\text{out}(n_1, \text{not}_1(x)), \text{in}(n_2, \text{and}_1(x)))$ $\text{cnf}(\text{halfadder_connection_out1not}_1_in2and}_1, \text{axiom})$

HWV001-2.ax Full-adder.

$\text{type}(x, \text{fulladder}) \Rightarrow \text{type}(h_1(x), \text{halfadder})$ $\text{cnf}(\text{fulladder_halfadder}_1, \text{axiom})$
 $\text{type}(x, \text{fulladder}) \Rightarrow \text{type}(h_2(x), \text{halfadder})$ $\text{cnf}(\text{fulladder_halfadder}_2, \text{axiom})$
 $\text{type}(x, \text{fulladder}) \Rightarrow \text{type}(\text{or}_1(x), \text{or})$ $\text{cnf}(\text{fulladder_or}_1, \text{axiom})$
 $\text{type}(x, \text{fulladder}) \Rightarrow \text{connection}(\text{out}(s, h_1(x)), \text{in}(n_2, h_2(x)))$ $\text{cnf}(\text{fulladder_connection_outsh}_1_in2h}_2, \text{axiom})$
 $\text{type}(x, \text{fulladder}) \Rightarrow \text{connection}(\text{out}(c, h_1(x)), \text{in}(n_2, \text{or}_1(x)))$ $\text{cnf}(\text{fulladder_connection_outch}_1_in2or}_1, \text{axiom})$
 $\text{type}(x, \text{fulladder}) \Rightarrow \text{connection}(\text{out}(c, h_2(x)), \text{in}(n_1, \text{or}_1(x)))$ $\text{cnf}(\text{fulladder_connection_outch}_2_in1or}_1, \text{axiom})$
 $\text{type}(x, \text{fulladder}) \Rightarrow \text{connection}(\text{in}(n_1, x), \text{in}(n_1, h_2(x)))$ $\text{cnf}(\text{fulladder_connection_in1_in1h}_2, \text{axiom})$
 $\text{type}(x, \text{fulladder}) \Rightarrow \text{connection}(\text{in}(n_2, x), \text{in}(n_1, h_1(x)))$ $\text{cnf}(\text{fulladder_connection_in2_in1h}_1, \text{axiom})$
 $\text{type}(x, \text{fulladder}) \Rightarrow \text{connection}(\text{in}(c, x), \text{in}(n_2, h_1(x)))$ $\text{cnf}(\text{fulladder_connection_inc_in2h}_1, \text{axiom})$
 $\text{type}(x, \text{fulladder}) \Rightarrow \text{connection}(\text{out}(s, x), \text{out}(s, h_2(x)))$ $\text{cnf}(\text{fulladder_connection_outs_outsh}_2, \text{axiom})$
 $\text{type}(x, \text{fulladder}) \Rightarrow \text{connection}(\text{out}(c, x), \text{out}(n_1, \text{or}_1(x)))$ $\text{cnf}(\text{fulladder_connection_outc_out1or}_1, \text{axiom})$

HWV002-0.ax Connections, faults, and gates.

$(\text{connection}(p_1, p_2) \text{ and } 0) \Rightarrow 0$ $\text{cnf}(\text{value_propagation_zero}_1, \text{axiom})$
 $(\text{connection}(p_1, p_2) \text{ and } 1) \Rightarrow 1$ $\text{cnf}(\text{value_propagation_one}_1, \text{axiom})$
 $(\text{connection}(p_1, p_2) \text{ and } 0) \Rightarrow 0$ $\text{cnf}(\text{value_propagation_zero}_2, \text{axiom})$
 $(\text{connection}(p_1, p_2) \text{ and } 1) \Rightarrow 1$ $\text{cnf}(\text{value_propagation_one}_2, \text{axiom})$
 $0 \Rightarrow \neg 1$ $\text{cnf}(\text{unique_value}, \text{axiom})$
 $(\text{and_ok}(k) \text{ and } 0) \Rightarrow 0$ $\text{cnf}(\text{and_0x}_0, \text{axiom})$

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(and_ok(k) and 0) => 0    cnf(and_x0_0, axiom)
(and_ok(k) and 1 and 1) => 1    cnf(and_11_1, axiom)
(and_ok(k) and 0) => (0 or 0)    cnf(and_0_0_0, axiom)
(and_ok(k) and 1) => 1    cnf(and_1_1_x, axiom)
(and_ok(k) and 1) => 1    cnf(and_1_x_1, axiom)
and_ok(k) => ¬ abnormal(k)    cnf(not_and_ok_and_abnormal, axiom)
logic_and(k) => (and_ok(k) or abnormal(k))    cnf(and_ok_or_abnormal, axiom)
(or_ok(k) and 1) => 1    cnf(or_1_x_1, axiom)
(or_ok(k) and 1) => 1    cnf(or_x_1_1, axiom)
(or_ok(k) and 0 and 0) => 0    cnf(or_0_0_0, axiom)
(or_ok(k) and 1) => (1 or 1)    cnf(or_1_1_1, axiom)
(or_ok(k) and 0) => 0    cnf(or_0_0_x, axiom)
(or_ok(k) and 0) => 0    cnf(or_0_0_1, axiom)
or_ok(k) => ¬ abnormal(k)    cnf(not_or_ok_and_abnormal, axiom)
logic_or(k) => (or_ok(k) or abnormal(k))    cnf(or_ok_or_abnormal, axiom)
(not_ok(k) and 0) => 1    cnf(not_0_1_fw, axiom)
(not_ok(k) and 1) => 0    cnf(not_1_0_fw, axiom)
(not_ok(k) and 0) => 1    cnf(not_0_1_bw, axiom)
(not_ok(k) and 1) => 0    cnf(not_1_0_bw, axiom)
not_ok(k) => ¬ abnormal(k)    cnf(not_not_ok_and_abnormal, axiom)
logic_not(k) => (not_ok(k) or abnormal(k))    cnf(not_ok_or_abnormal, axiom)

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HWV002-1.ax Half-adder.

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halfadder(x) => logic_and(and_1(x))    cnf(halfadder_and_1, axiom)
halfadder(x) => logic_and(and_2(x))    cnf(halfadder_and_2, axiom)
halfadder(x) => logic_not(not_1(x))    cnf(halfadder_not_1, axiom)
halfadder(x) => logic_or(or_1(x))    cnf(halfadder_or_1, axiom)
halfadder(x) => connection(in_1(x), in_1(or_1(x)))    cnf(halfadder_connection_in1_in1or1, axiom)
halfadder(x) => connection(in_2(x), in_2(or_1(x)))    cnf(halfadder_connection_in2_in2or1, axiom)
halfadder(x) => connection(in_1(x), in_1(and_2(x)))    cnf(halfadder_connection_in1_in1and2, axiom)
halfadder(x) => connection(in_2(x), in_2(and_2(x)))    cnf(halfadder_connection_in2_in2and2, axiom)
halfadder(x) => connection(outs(x), out_1(and_1(x)))    cnf(halfadder_connection_outs_out1and1, axiom)
halfadder(x) => connection(outc(x), out_1(and_2(x)))    cnf(halfadder_connection_outc_out1and2, axiom)
halfadder(x) => connection(out_1(or_1(x)), in_1(and_1(x)))    cnf(halfadder_connection_out1or1_in1and1, axiom)
halfadder(x) => connection(out_1(and_2(x)), in_1(not_1(x)))    cnf(halfadder_connection_out1and2_in1not1, axiom)
halfadder(x) => connection(out_1(not_1(x)), in_2(and_1(x)))    cnf(halfadder_connection_out1not1_in2and1, axiom)

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HWV002-2.ax Full-adder.

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fulladder(x) => halfadder(h_1(x))    cnf(fulladder_halfadder_1, axiom)
fulladder(x) => halfadder(h_2(x))    cnf(fulladder_halfadder_2, axiom)
fulladder(x) => logic_or(or_1(x))    cnf(fulladder_or_1, axiom)
fulladder(x) => connection(outs(h_1(x)), in_2(h_2(x)))    cnf(fulladder_connection_outsh1_in2h2, axiom)
fulladder(x) => connection(outc(h_1(x)), in_2(or_1(x)))    cnf(fulladder_connection_outch1_in2or1, axiom)
fulladder(x) => connection(outc(h_2(x)), in_1(or_1(x)))    cnf(fulladder_connection_outch2_in1or1, axiom)
fulladder(x) => connection(in_1(x), in_1(h_2(x)))    cnf(fulladder_connection_in1_in1h2, axiom)
fulladder(x) => connection(in_2(x), in_1(h_1(x)))    cnf(fulladder_connection_in2_in1h1, axiom)
fulladder(x) => connection(inc(x), in_2(h_1(x)))    cnf(fulladder_connection_inc_in2h1, axiom)
fulladder(x) => connection(outs(x), outs(h_2(x)))    cnf(fulladder_connection_outs_outsh2, axiom)
fulladder(x) => connection(outc(x), out_1(or_1(x)))    cnf(fulladder_connection_outc_out1or1, axiom)

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HWV problems

HWV001-1.p Interchange inputs to outputs

This validates one of the circuit designs that will take x and y as input and output y and x without crossing any wires.

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include('Axioms/HWC002-0.ax')
and(x, y) = and(y, x)    cnf(and_commutativity, axiom)
or(x, y) = or(y, x)    cnf(or_commutativity, axiom)
and(x, and(y, z)) = and(and(x, y), z)    cnf(and_associativity, axiom)
or(x, or(y, z)) = or(or(x, y), z)    cnf(or_associativity, axiom)

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or(or(x, y), z) = or(or(x, z), y)    cnf(or_sorting, axiom)
and(and(x, y), z) = and(and(x, z), y)  cnf(and_sorting, axiom)
not(and(x, y)) = or(not(x), not(y))    cnf(not_canonicalization1, axiom)
not(or(x, y)) = and(not(x), not(y))    cnf(not_canonicalization2, axiom)
and(or(x, y), z) = or(and(x, z), and(y, z))  cnf(and_or_canonicalization, axiom)
and(x, x) = x                          cnf(and_simplification1, axiom)
and(and(x, y), y) = and(x, y)         cnf(and_simplification2, axiom)
and(and(x, y), x) = and(x, y)         cnf(and_simplification3, axiom)
or(x, x) = x                           cnf(or_simplification1, axiom)
or(or(x, y), y) = or(x, y)           cnf(or_simplification2, axiom)
or(or(x, y), x) = or(x, y)           cnf(or_simplification3, axiom)
and(x, not(x)) = n0                   cnf(and_not_simplification1, axiom)
and(and(x, y), not(y)) = n0          cnf(and_not_simplification2, axiom)
and(and(x, y), not(x)) = n0          cnf(and_not_simplification3, axiom)
or(x, not(x)) = n1                    cnf(or_not_simplification1, axiom)
or(or(x, y), not(y)) = n1            cnf(or_not_simplification2, axiom)
or(or(x, y), not(x)) = n1            cnf(or_not_simplification3, axiom)
not(not(x)) = x                       cnf(not_simplification, axiom)
or(and(x, y), and(x, not(y))) = x     cnf(and_or_not_simplification1, axiom)
or(and(x, y), and(y, not(x))) = y     cnf(and_or_not_simplification2, axiom)
a1 = and(b1, b3)                      cnf(constructor1, negated_conjecture)
a2 = and(b2, b3)                      cnf(constructor2, negated_conjecture)
b1 = not(d1)                          cnf(constructor3, negated_conjecture)
b2 = not(d2)                          cnf(constructor4, negated_conjecture)
b3 = or(c1, c2)                       cnf(constructor5, negated_conjecture)
c1 = or(d1, d3)                       cnf(constructor6, negated_conjecture)
c2 = or(d2, d3)                       cnf(constructor7, negated_conjecture)
d3 = f3                                cnf(constructor8, negated_conjecture)
d1 = not(e1)                          cnf(constructor9, negated_conjecture)
d2 = not(e2)                          cnf(constructor10, negated_conjecture)
e1 = or(f1, f3)                       cnf(constructor11, negated_conjecture)
e2 = or(f2, f3)                       cnf(constructor12, negated_conjecture)
f1 = not(i1)                          cnf(constructor13, negated_conjecture)
f2 = not(i2)                          cnf(constructor14, negated_conjecture)
f3 = and(i1, i2)                      cnf(constructor15, negated_conjecture)
circuit(input(i1, i2), output(a1, a2))  cnf(circuit_description, negated_conjecture)
¬ circuit(input(i1, i2), output(i2, i1))  cnf(prove_interchange, negated_conjecture)

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HWV003-1.p One bit Full Adder

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include('Axioms/HWC002-0.ax')
not(and(x, y)) = or(not(x), not(y))    cnf(demorgan1, axiom)
not(or(x, y)) = and(not(x), not(y))    cnf(demorgan2, axiom)
not(not(x)) = x                       cnf(not_involution, axiom)
and(x, y) = and(y, x)                 cnf(and_symmetry, negated_conjecture)
or(x, y) = or(y, x)                   cnf(or_symmetry, negated_conjecture)
and(or(x, y), z) = or(and(x, z), and(y, z))  cnf(and_or_simplification, negated_conjecture)
and(and(x, y), z) = and(and(x, z), y)  cnf(and_commutativity, negated_conjecture)
or(or(x, y), z) = or(or(x, z), y)     cnf(or_commutativity, negated_conjecture)
and(x, not(x)) = n0                   cnf(and_not_evaluation1, axiom)
or(x, not(x)) = n1                    cnf(or_not_evaluation1, axiom)
and(x, x) = x                         cnf(and_idempotency, axiom)
or(x, x) = x                          cnf(or_idempotency, axiom)
and(and(x, y), not(y)) = n0           cnf(and_not_evaluation2, axiom)
and(and(x, y), not(x)) = n0           cnf(and_not_evaluation3, axiom)
or(or(x, y), not(y)) = n1             cnf(or_not_evaluation2, axiom)
or(or(x, y), not(x)) = n1            cnf(or_not_evaluation3, axiom)
and(and(x, y), y) = and(x, y)         cnf(and_evaluation1, axiom)
or(or(x, y), y) = or(x, y)           cnf(or_evaluation1, axiom)
and(and(and(x1, x2), x3), not(x1)) = n0  cnf(and_not_evaluation4, axiom)
and(and(and(x1, x2), x3), not(x2)) = n0  cnf(and_not_evaluation5, axiom)

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$\text{or}(\text{and}(x, y), y) = y$ $\text{cnf}(\text{and_or_subsumption}_1, \text{axiom})$
 $\text{or}(\text{and}(x, y), x) = x$ $\text{cnf}(\text{and_or_subsumption}_2, \text{axiom})$
 $\text{or}(\text{or}(\text{and}(x, y), z), y) = \text{or}(z, y)$ $\text{cnf}(\text{and_or_subsumption}_3, \text{axiom})$
 $\text{or}(\text{or}(x, \text{and}(y, z)), z) = \text{or}(x, z)$ $\text{cnf}(\text{and_or_subsumption}_4, \text{axiom})$
 $\text{or}(\text{and}(x, \text{not}(y)), y) = \text{or}(x, y)$ $\text{cnf}(\text{karnaugh}_1, \text{axiom})$
 $\text{or}(\text{and}(\text{not}(x), \text{not}(y)), y) = \text{or}(y, \text{not}(x))$ $\text{cnf}(\text{karnaugh}_2, \text{axiom})$
 $\text{or}(\text{and}(\text{and}(x, y), \text{not}(z)), \text{and}(x, z)) = \text{or}(\text{and}(x, y), \text{and}(x, z))$ $\text{cnf}(\text{karnaugh}_3, \text{axiom})$
 $\text{xor}(x, y) = \text{or}(\text{and}(x, \text{not}(y)), \text{and}(y, \text{not}(x)))$ $\text{cnf}(\text{xor_definition}, \text{axiom})$
 $\text{carryout}(x, y, z) = \text{or}(\text{and}(x, \text{or}(y, z)), \text{and}(\text{not}(x), \text{and}(y, z)))$ $\text{cnf}(\text{carryout_definition}, \text{negated_conjecture})$
 $x + y = z = \text{xor}(\text{xor}(x, y), z)$ $\text{cnf}(\text{sum_definition}, \text{negated_conjecture})$
 $a_{11} = \text{not}(\text{and}(a, b))$ $\text{cnf}(\text{circuit}_1, \text{negated_conjecture})$
 $a_{12} = \text{not}(\text{and}(a_{11}, a))$ $\text{cnf}(\text{circuit}_2, \text{negated_conjecture})$
 $a_{13} = \text{not}(\text{and}(a_{11}, b))$ $\text{cnf}(\text{circuit}_3, \text{negated_conjecture})$
 $a_{14} = \text{not}(\text{and}(a_{12}, a_{13}))$ $\text{cnf}(\text{circuit}_4, \text{negated_conjecture})$
 $a_{15} = \text{not}(\text{and}(a_{14}, \text{carryin}))$ $\text{cnf}(\text{circuit}_5, \text{negated_conjecture})$
 $a_{16} = \text{not}(\text{and}(a_{14}, a_{15}))$ $\text{cnf}(\text{circuit}_6, \text{negated_conjecture})$
 $a_{17} = \text{not}(\text{and}(a_{15}, \text{carryin}))$ $\text{cnf}(\text{circuit}_7, \text{negated_conjecture})$
 $s_1 = \text{not}(\text{and}(a_{16}, a_{17}))$ $\text{cnf}(\text{circuit}_8, \text{negated_conjecture})$
 $c_1 = \text{not}(\text{and}(a_{11}, a_{15}))$ $\text{cnf}(\text{circuit}_9, \text{negated_conjecture})$
 $\text{circuit}(s_1, c_1)$ $\text{cnf}(\text{the_output_circuit}, \text{negated_conjecture})$
 $\neg \text{circuit}(a + b = \text{carryin}, \text{carryout}(a, b, \text{carryin}))$ $\text{cnf}(\text{prove_circuit}, \text{negated_conjecture})$

HWV003-2.p One bit Full Adder

Prove that the given implementation of a one-bit full adder using only NAND gates is correct

$\text{or}(x, y) = \text{or}(y, x)$ $\text{cnf}(\text{or_commutative}, \text{axiom})$
 $\text{and}(x, y) = \text{and}(y, x)$ $\text{cnf}(\text{and_commutative}, \text{axiom})$
 $\text{or}(\text{or}(x, y), z) = \text{or}(x, \text{or}(y, z))$ $\text{cnf}(\text{or_associative}, \text{axiom})$
 $\text{and}(\text{and}(x, y), z) = \text{and}(x, \text{and}(y, z))$ $\text{cnf}(\text{and_associative}, \text{axiom})$
 $\text{or}(x, \text{ll}_0) = x$ $\text{cnf}(\text{or_identity}, \text{axiom})$
 $\text{and}(x, \text{ll}_1) = x$ $\text{cnf}(\text{and_identity}, \text{axiom})$
 $\text{and}(x, \text{or}(y, z)) = \text{or}(\text{and}(x, y), \text{and}(x, z))$ $\text{cnf}(\text{or_distributive}, \text{axiom})$
 $\text{or}(x, \text{and}(y, z)) = \text{and}(\text{or}(x, y), \text{or}(x, z))$ $\text{cnf}(\text{and_distributive}, \text{axiom})$
 $\text{or}(x, \text{not}(x)) = \text{ll}_1$ $\text{cnf}(\text{or_complement}, \text{axiom})$
 $\text{and}(x, \text{not}(x)) = \text{ll}_0$ $\text{cnf}(\text{and_complement}, \text{axiom})$
 $\text{or}(x, x) = x$ $\text{cnf}(\text{or_idempotent}, \text{axiom})$
 $\text{and}(x, x) = x$ $\text{cnf}(\text{and_idempotent}, \text{axiom})$
 $\text{not}(\text{not}(x)) = x$ $\text{cnf}(\text{not_involution}, \text{axiom})$
 $\text{not}(\text{ll}_0) = \text{ll}_1$ $\text{cnf}(\text{ll0_inverse}, \text{axiom})$
 $\text{not}(\text{ll}_1) = \text{ll}_0$ $\text{cnf}(\text{ll1_inverse}, \text{axiom})$
 $\text{or}(x, \text{ll}_1) = \text{ll}_1$ $\text{cnf}(\text{or_boundedness}, \text{axiom})$
 $\text{and}(x, \text{ll}_0) = \text{ll}_0$ $\text{cnf}(\text{and_boundedness}, \text{axiom})$
 $\text{or}(x, \text{and}(x, y)) = x$ $\text{cnf}(\text{or_absorption}, \text{axiom})$
 $\text{and}(x, \text{or}(x, y)) = x$ $\text{cnf}(\text{and_absorption}, \text{axiom})$
 $\text{not}(\text{or}(x, y)) = \text{and}(\text{not}(x), \text{not}(y))$ $\text{cnf}(\text{or_demorgan}, \text{axiom})$
 $\text{not}(\text{and}(x, y)) = \text{or}(\text{not}(x), \text{not}(y))$ $\text{cnf}(\text{and_demorgan}, \text{axiom})$
 $\text{or}(\text{and}(\text{not}(x), y), \text{and}(x, \text{not}(y))) = \text{xor}(x, y)$ $\text{cnf}(\text{xor_definition}, \text{axiom})$
 $\text{xor}(x, y) = \text{xor}(y, x)$ $\text{cnf}(\text{xor_commutative}, \text{axiom})$
 $\text{xor}(x, \text{xor}(y, z)) = \text{xor}(\text{xor}(x, y), z)$ $\text{cnf}(\text{xor_associative}, \text{axiom})$
 $\text{xor}(\text{xor}(a, b), \text{cin}) = \text{sum_def}$ $\text{cnf}(\text{sum_def}, \text{negated_conjecture})$
 $\text{or}(\text{and}(\text{cin}, \text{or}(a, b)), \text{and}(\text{not}(\text{cin}), \text{and}(a, b))) = \text{carry_def}$ $\text{cnf}(\text{carry_def}, \text{negated_conjecture})$
 $\text{not}(\text{and}(a, b)) = t_1$ $\text{cnf}(t_1, \text{negated_conjecture})$
 $\text{not}(\text{and}(a, t_1)) = t_2$ $\text{cnf}(t_2, \text{negated_conjecture})$
 $\text{not}(\text{and}(b, t_1)) = t_3$ $\text{cnf}(t_3, \text{negated_conjecture})$
 $\text{not}(\text{and}(t_2, t_3)) = t_4$ $\text{cnf}(t_4, \text{negated_conjecture})$
 $\text{not}(\text{and}(t_4, \text{cin})) = t_5$ $\text{cnf}(t_5, \text{negated_conjecture})$
 $\text{not}(\text{and}(t_4, t_5)) = t_6$ $\text{cnf}(t_6, \text{negated_conjecture})$
 $\text{not}(\text{and}(t_5, \text{cin})) = t_7$ $\text{cnf}(t_7, \text{negated_conjecture})$
 $\text{not}(\text{and}(t_6, t_7)) = +$ $\text{cnf}(\text{sum}, \text{negated_conjecture})$
 $\text{not}(\text{and}(t_1, t_5)) = \text{carry}$ $\text{cnf}(\text{carry}, \text{negated_conjecture})$
 $+ = \text{sum_def} \Rightarrow \text{carry} \neq \text{carry_def}$ $\text{cnf}(\text{prove_circuit}, \text{negated_conjecture})$

HWV004-1.p Two bit Full Adder

```

include('Axioms/HWC002-0.ax')
not(and(x,y)) = or(not(x),not(y))    cnf(demorgan1, axiom)
not(or(x,y)) = and(not(x),not(y))    cnf(demorgan2, axiom)
not(not(x)) = x                      cnf(not_involution, axiom)
and(x,y) = and(y,x)                  cnf(and_symmetry, negated_conjecture)
or(x,y) = or(y,x)                     cnf(or_symmetry, negated_conjecture)
and(or(x,y),z) = or(and(x,z),and(y,z))  cnf(and_or_simplification, negated_conjecture)
and(and(x,y),z) = and(and(x,z),y)      cnf(and_commutativity, negated_conjecture)
or(or(x,y),z) = or(or(x,z),y)         cnf(or_commutativity, negated_conjecture)
and(x,not(x)) = n0                    cnf(and_not_evaluation1, axiom)
or(x,not(x)) = n1                     cnf(or_not_evaluation1, axiom)
and(x,x) = x                          cnf(and_idempotency, axiom)
or(x,x) = x                            cnf(or_idempotency, axiom)
and(and(x,y),not(y)) = n0              cnf(and_not_evaluation2, axiom)
and(and(x,y),not(x)) = n0              cnf(and_not_evaluation3, axiom)
or(or(x,y),not(y)) = n1                cnf(or_not_evaluation2, axiom)
or(or(x,y),not(x)) = n1                cnf(or_not_evaluation3, axiom)
and(and(x,y),y) = and(x,y)            cnf(and_evaluation1, axiom)
or(or(x,y),y) = or(x,y)               cnf(or_evaluation1, axiom)
and(and(and(x1,x2),x3),not(x1)) = n0   cnf(and_not_evaluation4, axiom)
and(and(and(x1,x2),x3),not(x2)) = n0   cnf(and_not_evaluation5, axiom)
or(and(x,y),y) = y                     cnf(and_or_subsumption1, axiom)
or(and(x,y),x) = x                     cnf(and_or_subsumption2, axiom)
or(or(and(x,y),z),y) = or(z,y)         cnf(and_or_subsumption3, axiom)
or(or(x,and(y,z)),z) = or(x,z)         cnf(and_or_subsumption4, axiom)
or(and(x,not(y)),y) = or(x,y)          cnf(karnaugh1, axiom)
or(and(not(x),not(y)),y) = or(y,not(x))  cnf(karnaugh2, axiom)
or(and(and(x,y),not(z)),and(x,z)) = or(and(x,y),and(x,z))  cnf(karnaugh3, axiom)
xor(x,y) = or(and(x,not(y)),and(y,not(x)))  cnf(xor_definition, axiom)
carryout(x,y,z) = or(and(x,or(y,z)),and(not(x),and(y,z)))  cnf(carryout_definition, negated_conjecture)
x + y = z = xor(xor(x,y),z)            cnf(sum_definition, negated_conjecture)
s0 = a0 + b0 = n0                      cnf(s0_definition, negated_conjecture)
s1 = a1 + b1 = carryout(a0,b0,n0)      cnf(s1_definition, negated_conjecture)
overflow = carryout(a1,b1,carryout(a0,b0,n0))  cnf(overflow_definition, negated_conjecture)
circuit(s0,s1,overflow)                cnf(the_output_circuit, negated_conjecture)
¬ circuit(xor(a0,b0),xor(xor(a1,b1),carryout(a0,b0,n0)),or(and(a1,b1),and(and(a0,b0),or(a1,b1))))  cnf(prove_circuit, negated_conjecture)

```

HWV005-1.p A halfadder built from and, or and not gates

```

include('Axioms/HWV001-0.ax')
include('Axioms/HWV001-1.ax')
type(h, halfadder)                    cnf(h_isa_halfadder, hypothesis)
value(in(n1,h),n1)                    cnf(in1, hypothesis)
value(in(n2,h),n0)                    cnf(in2, hypothesis)
value(out(s,h),n0)                    cnf(outs0, hypothesis)
value(out(c,h),n0)                    cnf(outc0, hypothesis)
¬ mode(and1(h),abnormal)               cnf(diagnosis_and1, negated_conjecture)
¬ mode(not1(h),abnormal)               cnf(diagnosis_not1, negated_conjecture)
¬ mode(or1(h),abnormal)                cnf(diagnosis_or1, negated_conjecture)

```

HWV005-2.p A halfadder built from and, or and not gates

```

include('Axioms/HWV002-0.ax')
include('Axioms/HWV002-1.ax')
halfadder(h)                          cnf(h_isa_halfadder, hypothesis)
1                                      cnf(in1, hypothesis)
0                                      cnf(in2, hypothesis)
0                                      cnf(outs0, hypothesis)
0                                      cnf(outc0, hypothesis)
¬ abnormal(and1(h))                    cnf(diagnosis_and1, negated_conjecture)
¬ abnormal(not1(h))                    cnf(diagnosis_not1, negated_conjecture)

```

\neg abnormal($\text{or}_1(h)$) cnf(diagnosis_or1, negated_conjecture)

HWV006-1.p A fulladder built from two halfadders and an or gate

include('Axioms/HWV001-0.ax')

include('Axioms/HWV001-1.ax')

include('Axioms/HWV001-2.ax')

type(f , fulladder) cnf(f .isa_fulladder, hypothesis)

value(in(n_1 , f), n_1) cnf(in1₁, hypothesis)

value(in(n_2 , f), n_0) cnf(in2₀, hypothesis)

value(in(c , f), n_1) cnf(inc₁, hypothesis)

value(out(s , f), n_1) cnf(outs₁, hypothesis)

value(out(c , f), n_0) cnf(outc₀, hypothesis)

mode($\text{or}_1(f)$, abnormal) \Rightarrow \neg mode(not₁($h_2(f)$), abnormal) cnf(diagnosis_or1_not1h₂, negated_conjecture)

\neg mode(and₂($h_2(f)$), abnormal) cnf(diagnosis_and2, negated_conjecture)

mode($\text{or}_1(f)$, abnormal) \Rightarrow \neg mode(and₁($h_2(f)$), abnormal) cnf(diagnosis_or1_and1h₂, negated_conjecture)

\neg mode($\text{or}_1(h_1(f))$, abnormal) cnf(diagnosis_or1h₁, negated_conjecture)

\neg mode(not₁($h_1(f)$), abnormal) cnf(diagnosis_not1h₁, negated_conjecture)

\neg mode(and₂($h_1(f)$), abnormal) cnf(diagnosis_and2h₁, negated_conjecture)

\neg mode(and₁($h_1(f)$), abnormal) cnf(diagnosis_and1h₁, negated_conjecture)

HWV006-2.p A fulladder built from two halfadders and an or gate

include('Axioms/HWV002-0.ax')

include('Axioms/HWV002-1.ax')

include('Axioms/HWV002-2.ax')

fulladder(f) cnf(f .isa_fulladder, hypothesis)

1 cnf(in1₁, hypothesis)

0 cnf(in2₀, hypothesis)

1 cnf(inc₁, hypothesis)

1 cnf(outs₁, hypothesis)

0 cnf(outc₀, hypothesis)

abnormal($\text{or}_1(f)$) \Rightarrow \neg abnormal(not₁($h_2(f)$)) cnf(diagnosis_or1_not1h₂, negated_conjecture)

\neg abnormal(and₂($h_2(f)$)) cnf(diagnosis_and2, negated_conjecture)

abnormal($\text{or}_1(f)$) \Rightarrow \neg abnormal(and₁($h_2(f)$)) cnf(diagnosis_or1_and1h₂, negated_conjecture)

\neg abnormal($\text{or}_1(h_1(f))$) cnf(diagnosis_or1h₁, negated_conjecture)

\neg abnormal(not₁($h_1(f)$)) cnf(diagnosis_not1h₁, negated_conjecture)

\neg abnormal(and₂($h_1(f)$)) cnf(diagnosis_and2h₁, negated_conjecture)

\neg abnormal(and₁($h_1(f)$)) cnf(diagnosis_and1h₁, negated_conjecture)

HWV007-1.p A fulladder built from two halfadders and an or gate

include('Axioms/HWV001-0.ax')

include('Axioms/HWV001-1.ax')

include('Axioms/HWV001-2.ax')

type(f , fulladder) cnf(f .isa_fulladder, hypothesis)

value(in(n_1 , f), n_0) cnf(in1₁, hypothesis)

value(in(n_2 , f), n_1) cnf(in2₀, hypothesis)

value(in(c , f), n_1) cnf(inc₁, hypothesis)

value(out(s , f), n_1) cnf(outs₁, hypothesis)

value(out(c , f), n_0) cnf(outc₀, hypothesis)

\neg mode(and₂($h_1(f)$), abnormal) cnf(diagnosis_and2h₁, negated_conjecture)

mode($\text{or}_1(f)$, abnormal) \Rightarrow \neg mode(and₁($h_1(f)$), abnormal) cnf(diagnosis_or1_and1h₁, negated_conjecture)

mode($\text{or}_1(f)$, abnormal) \Rightarrow \neg mode(not₁($h_1(f)$), abnormal) cnf(diagnosis_or1_not1h₁, negated_conjecture)

mode($\text{or}_1(f)$, abnormal) \Rightarrow \neg mode(and₁($h_2(f)$), abnormal) cnf(diagnosis_or1_and1h₂, negated_conjecture)

mode($\text{or}_1(f)$, abnormal) \Rightarrow \neg mode($\text{or}_1(h_2(f))$, abnormal) cnf(diagnosis_or1_or1h₂, negated_conjecture)

HWV007-2.p A fulladder built from two halfadders and an or gate

include('Axioms/HWV002-0.ax')

include('Axioms/HWV002-1.ax')

include('Axioms/HWV002-2.ax')

fulladder(f) cnf(f .isa_fulladder, hypothesis)

0 cnf(in1₁, hypothesis)

1 cnf(in2₀, hypothesis)

```

1   cnf(inc1, hypothesis)
1   cnf(outs1, hypothesis)
0   cnf(outc0, hypothesis)
¬ abnormal(and2(h1(f)))   cnf(diagnosis_and2h1, negated_conjecture)
abnormal(or1(f)) ⇒ ¬ abnormal(and1(h1(f)))   cnf(diagnosis_or1_and1h1, negated_conjecture)
abnormal(or1(f)) ⇒ ¬ abnormal(not1(h1(f)))   cnf(diagnosis_or1_not1h1, negated_conjecture)
abnormal(or1(f)) ⇒ ¬ abnormal(and1(h2(f)))   cnf(diagnosis_or1_and1h2, negated_conjecture)
abnormal(or1(f)) ⇒ ¬ abnormal(or1(h2(f)))   cnf(diagnosis_or1_or1h2, negated_conjecture)

```

HWV008-1.001.p 1 bit ripple carry adder

```

include('Axioms/HWV001-0.ax')
include('Axioms/HWV001-1.ax')
include('Axioms/HWV001-2.ax')
type(x, nbit_adder(n1)) ⇒ type(v(n1, x), fulladder)   cnf(nbit_adder_fulladder1, axiom)
type(x, nbit_adder(n1)) ⇒ connection(out(n1, x), out(s, v(n1, x)))   cnf(nbit_adder_connection_out1_out1v1, axiom)
type(x, nbit_adder(n1)) ⇒ connection(out(c, x), out(c, v(n1, x)))   cnf(nbit_adder_connection_outc_outcv1, axiom)
type(x, nbit_adder(n1)) ⇒ connection(in(a1, x), in(n1, v(n1, x)))   cnf(nbit_adder_connection_ina1_in1v1, axiom)
type(x, nbit_adder(n1)) ⇒ connection(in(b1, x), in(n2, v(n1, x)))   cnf(nbit_adder_connection_inb1_in2v1, axiom)
type(x, nbit_adder(n1)) ⇒ connection(in(c, x), in(c, v(n1, x)))   cnf(nbit_adder_connection_inc_incv1, axiom)
type(a, nbit_adder(n1))   cnf(a_isa_1bit_adder, hypothesis)
value(in(a1, a), n0)   cnf(ina10, hypothesis)
value(in(b1, a), n0)   cnf(inb10, hypothesis)
value(in(c, a), n0)   cnf(inc0, hypothesis)
value(out(n1, a), n0)   cnf(out10, hypothesis)
value(out(c, a), n1)   cnf(outc0, hypothesis)
¬ mode(or1(v(n1, a)), abnormal)   cnf(diagnosis_or1v1, negated_conjecture)
¬ mode(and2(h1(v(n1, a))), abnormal)   cnf(diagnosis_and2h1v1, negated_conjecture)
¬ mode(and2(h2(v(n1, a))), abnormal)   cnf(diagnosis_and2h2v1, negated_conjecture)

```

HWV008-1.002.p 2 bit ripple carry adder

```

include('Axioms/HWV001-0.ax')
include('Axioms/HWV001-1.ax')
include('Axioms/HWV001-2.ax')
type(x, nbit_adder(n2)) ⇒ type(f(n1, x), fulladder)   cnf(nbit_adder_fulladder1, axiom)
type(x, nbit_adder(n2)) ⇒ type(f(n2, x), fulladder)   cnf(nbit_adder_fulladder2, axiom)
type(x, nbit_adder(n2)) ⇒ connection(out(n1, x), out(n1, f(n1, x)))   cnf(nbit_adder_connection_out1_out1f1, axiom)
type(x, nbit_adder(n2)) ⇒ connection(out(n2, x), out(n1, f(n2, x)))   cnf(nbit_adder_connection_out2_out1f2, axiom)
type(x, nbit_adder(n2)) ⇒ connection(out(c, x), out(c, f(n2, x)))   cnf(nbit_adder_connection_outc_outcf1, axiom)
type(x, nbit_adder(n2)) ⇒ connection(in(a1, x), in(n1, f(n1, x)))   cnf(nbit_adder_connection_ina1_in1f1, axiom)
type(x, nbit_adder(n2)) ⇒ connection(in(b1, x), in(n2, f(n1, x)))   cnf(nbit_adder_connection_inb1_in2f1, axiom)
type(x, nbit_adder(n2)) ⇒ connection(in(a2, x), in(n1, f(n2, x)))   cnf(nbit_adder_connection_ina2_in1f2, axiom)
type(x, nbit_adder(n2)) ⇒ connection(in(b2, x), in(n2, f(n2, x)))   cnf(nbit_adder_connection_inb2_in2f2, axiom)
type(x, nbit_adder(n2)) ⇒ connection(out(c, f(n1, x)), in(c, f(n2, x)))   cnf(nbit_adder_connection_inc_incf1, axiom)
type(x, nbit_adder(n2)) ⇒ connection(in(c, x), in(c, f(n1, x)))   cnf(nbit_adder_connection_inc_incf2, axiom)
type(a, nbit_adder(n2))   cnf(a_isa_2bit_adder, hypothesis)
value(in(a1, a), n0)   cnf(ina10, hypothesis)
value(in(a2, a), n0)   cnf(ina20, hypothesis)
value(in(b1, a), n0)   cnf(inb10, hypothesis)
value(in(b2, a), n0)   cnf(inb20, hypothesis)
value(in(c, a), n0)   cnf(inc0, hypothesis)
value(out(n1, a), n0)   cnf(out10, hypothesis)
value(out(n2, a), n0)   cnf(out20, hypothesis)
value(out(c, a), n1)   cnf(outc1, hypothesis)
¬ mode(or1(f(n2, a)), abnormal)   cnf(diagnosis_or1f2a, negated_conjecture)
¬ mode(and2(h1(f(n2, a))), abnormal)   cnf(diagnosis_and2h2f2a, negated_conjecture)
¬ mode(and2(h2(f(n2, a))), abnormal)   cnf(diagnosis_and2h1f2a, negated_conjecture)

```

HWV008-2.001.p 1 bit ripple carry adder

```

include('Axioms/HWV002-0.ax')
include('Axioms/HWV002-1.ax')
include('Axioms/HWV002-2.ax')

```

```

nbit_adder1(x) ⇒ fulladder(f1(x))    cnf(nbit_adder_fulladder1, axiom)
nbit_adder1(x) ⇒ connection(out1(x), outs(f1(x)))    cnf(nbit_adder_connection_out1_out1f1, axiom)
nbit_adder1(x) ⇒ connection(outc(x), outc(f1(x)))    cnf(nbit_adder_connection_outc_outcf1, axiom)
nbit_adder1(x) ⇒ connection(ina1(x), in1(f1(x)))    cnf(nbit_adder_connection_ina1_in1f1, axiom)
nbit_adder1(x) ⇒ connection(inb1(x), in2(f1(x)))    cnf(nbit_adder_connection_inb1_in2f1, axiom)
nbit_adder1(x) ⇒ connection(inc(x), inc(f1(x)))    cnf(nbit_adder_connection_inc_incf1, axiom)
nbit_adder1(a)    cnf(a_isa_1bit_adder, hypothesis)
0    cnf(ina10, hypothesis)
0    cnf(inb10, hypothesis)
0    cnf(inc0, hypothesis)
0    cnf(out10, hypothesis)
1    cnf(outc0, hypothesis)
¬ abnormal(or1(f1(a)))    cnf(diagnosis_or1f1, negated_conjecture)
¬ abnormal(and2(h1(f1(a))))    cnf(diagnosis_and2h1f1, negated_conjecture)
¬ abnormal(and2(h2(f1(a))))    cnf(diagnosis_and2h2f1, negated_conjecture)

```

HWV008-2.002.p 2 bit ripple carry adder

```

include('Axioms/HWV002-0.ax')
include('Axioms/HWV002-1.ax')
include('Axioms/HWV002-2.ax')
nbit_adder2(x) ⇒ fulladder(f1(x))    cnf(nbit_adder_fulladder1, axiom)
nbit_adder2(x) ⇒ fulladder(f2(x))    cnf(nbit_adder_fulladder2, axiom)
nbit_adder2(x) ⇒ connection(out1(x), out1(f1(x)))    cnf(nbit_adder_connection_out1_out1f1, axiom)
nbit_adder2(x) ⇒ connection(out2(x), out1(f2(x)))    cnf(nbit_adder_connection_out2_out1f2, axiom)
nbit_adder2(x) ⇒ connection(outc(x), outc(f2(x)))    cnf(nbit_adder_connection_outc_outcf1, axiom)
nbit_adder2(x) ⇒ connection(ina1(x), in1(f1(x)))    cnf(nbit_adder_connection_ina1_in1f1, axiom)
nbit_adder2(x) ⇒ connection(inb1(x), in2(f1(x)))    cnf(nbit_adder_connection_inb1_in2f1, axiom)
nbit_adder2(x) ⇒ connection(ina2(x), in1(f2(x)))    cnf(nbit_adder_connection_ina2_in1f2, axiom)
nbit_adder2(x) ⇒ connection(inb2(x), in2(f2(x)))    cnf(nbit_adder_connection_inb2_in2f2, axiom)
nbit_adder2(x) ⇒ connection(outc(f1(x)), inc(f2(x)))    cnf(nbit_adder_connection_inc_incf1, axiom)
nbit_adder2(x) ⇒ connection(inc(x), inc(f1(x)))    cnf(nbit_adder_connection_inc_incf2, axiom)
nbit_adder2(a)    cnf(a_isa_2bit_adder, hypothesis)
0    cnf(ina10, hypothesis)
0    cnf(ina20, hypothesis)
0    cnf(inb10, hypothesis)
0    cnf(inb20, hypothesis)
0    cnf(inc0, hypothesis)
0    cnf(out10, hypothesis)
0    cnf(out20, hypothesis)
1    cnf(outc1, hypothesis)
¬ abnormal(or1(f2(a)))    cnf(diagnosis_or1f2a, negated_conjecture)
¬ abnormal(and2(h1(f2(a))))    cnf(diagnosis_and2h1f2a, negated_conjecture)
¬ abnormal(and2(h2(f2(a))))    cnf(diagnosis_and2h2f2a, negated_conjecture)

```

HWV009-1.p Safelogic VHDL design verification obligation

```

include('Axioms/HWV003-0.ax')
p_Reset(t139)    cnf(quest1, negated_conjecture)
level(t139 + n1) = n0 ⇒ (p_Wr_error(t139 + n1) or p_Rd_error(t139 + n1))    cnf(quest2, negated_conjecture)

```

HWV009-2.p Safelogic VHDL design verification obligation

```

include('Axioms/HWV004-0.ax')
p_pred_(fwork_DOTfifo_DOTrtl_DOTreset_(t206))    cnf(quest1, negated_conjecture)
fwork_DOTfifo_DOTrtl_DOTlevel_(f_ADD_(t206, n1)) ≠ n0    cnf(quest2, negated_conjecture)

```

HWV009-3.p Safelogic VHDL design verification obligation

```

include('Axioms/HWV004-0.ax')
p_pred_(fwork_DOTfifo_DOTrtl_DOTreset_(t206))    cnf(quest1, negated_conjecture)
p_pred_(fwork_DOTfifo_DOTrtl_DOTwr_error_(f_ADD_(t206, n1)))    cnf(quest2, negated_conjecture)

```

HWV009-4.p Safelogic VHDL design verification obligation

```

include('Axioms/HWV004-0.ax')
p_pred_(fwork_DOTfifo_DOTrtl_DOTreset_(t206))    cnf(quest1, negated_conjecture)

```


$p_pred_(\text{fwork_DOTfifo_DOTrtl_DOTrd_error_}(f_ADD_(\text{t}_{206}, n_1))) \quad \text{cnf}(\text{quest}_2, \text{negated_conjecture})$

HWV010-1.p Safelogic VHDL design verification obligation

include('Axioms/HWV003-0.ax')

$p_Empty(\text{t}_{139}) \Rightarrow \text{level}(\text{t}_{139}) \neq n_0 \quad \text{cnf}(\text{quest}_1, \text{negated_conjecture})$

$p_Empty(\text{t}_{139}) \text{ or } \text{level}(\text{t}_{139}) = n_0 \quad \text{cnf}(\text{quest}_2, \text{negated_conjecture})$

HWV010-2.p Safelogic VHDL design verification obligation

include('Axioms/HWV004-0.ax')

$\text{fwork_DOTfifo_DOTrtl_DOTlevel_}(\text{t}_{206}) \neq n_0 \quad \text{cnf}(\text{quest}_1, \text{negated_conjecture})$

$p_pred_(\text{fwork_DOTfifo_DOTrtl_DOTempty_}(\text{t}_{206})) \quad \text{cnf}(\text{quest}_2, \text{negated_conjecture})$

HWV010-3.p Safelogic VHDL design verification obligation

include('Axioms/HWV004-0.ax')

$\text{fwork_DOTfifo_DOTrtl_DOTlevel_}(\text{t}_{206}) = n_0 \quad \text{cnf}(\text{quest}_1, \text{negated_conjecture})$

$\neg p_pred_(\text{fwork_DOTfifo_DOTrtl_DOTempty_}(\text{t}_{206})) \quad \text{cnf}(\text{quest}_2, \text{negated_conjecture})$

HWV011-1.p Safelogic VHDL design verification obligation

include('Axioms/HWV003-0.ax')

$p_Full(\text{t}_{139}) \Rightarrow \text{level}(\text{t}_{139}) \neq \text{fifo_length} \quad \text{cnf}(\text{quest}_1, \text{negated_conjecture})$

$p_Full(\text{t}_{139}) \text{ or } \text{level}(\text{t}_{139}) = \text{fifo_length} \quad \text{cnf}(\text{quest}_2, \text{negated_conjecture})$

HWV011-2.p Safelogic VHDL design verification obligation

include('Axioms/HWV004-0.ax')

$\text{fwork_DOTfifo_DOTrtl_DOTlevel_}(\text{t}_{206}) \neq \text{fwork_DOTfifo_DOTrtl_DOTfifo_length_} \quad \text{cnf}(\text{quest}_1, \text{negated_conjecture})$

$p_pred_(\text{fwork_DOTfifo_DOTrtl_DOTfull_}(\text{t}_{206})) \quad \text{cnf}(\text{quest}_2, \text{negated_conjecture})$

HWV011-3.p Safelogic VHDL design verification obligation

include('Axioms/HWV004-0.ax')

$\text{fwork_DOTfifo_DOTrtl_DOTlevel_}(\text{t}_{206}) = \text{fwork_DOTfifo_DOTrtl_DOTfifo_length_} \quad \text{cnf}(\text{quest}_1, \text{negated_conjecture})$

$\neg p_pred_(\text{fwork_DOTfifo_DOTrtl_DOTfull_}(\text{t}_{206})) \quad \text{cnf}(\text{quest}_2, \text{negated_conjecture})$

HWV012-1.p Safelogic VHDL design verification obligation

include('Axioms/HWV003-0.ax')

$gt(\text{fifo_length}, \text{level}(\text{t}_{139})) \quad \text{cnf}(\text{quest}_1, \text{negated_conjecture})$

$p_Wr(\text{t}_{139}) \quad \text{cnf}(\text{quest}_2, \text{negated_conjecture})$

$p_Wr_error(\text{t}_{139} + n_1) \quad \text{cnf}(\text{quest}_3, \text{negated_conjecture})$

HWV012-2.p Safelogic VHDL design verification obligation

include('Axioms/HWV004-0.ax')

$\neg p_LES_EQU_(\text{fwork_DOTfifo_DOTrtl_DOTfifo_length_}, \text{fwork_DOTfifo_DOTrtl_DOTlevel_}(\text{t}_{206})) \quad \text{cnf}(\text{quest}_1, \text{negated_conjecture})$

$p_pred_(\text{fwork_DOTfifo_DOTrtl_DOTwr_}(\text{t}_{206})) \quad \text{cnf}(\text{quest}_2, \text{negated_conjecture})$

$p_pred_(\text{fwork_DOTfifo_DOTrtl_DOTwr_error_}(f_ADD_(\text{t}_{206}, n_1))) \quad \text{cnf}(\text{quest}_3, \text{negated_conjecture})$

HWV013-1.p Safelogic VHDL design verification obligation

include('Axioms/HWV003-0.ax')

$\neg p_Reset(x_{139}) \quad \text{cnf}(\text{quest}_1, \text{negated_conjecture})$

$gt(\text{fifo_length}, \text{level}(x_{139})) \quad \text{cnf}(\text{quest}_2, \text{negated_conjecture})$

$\neg p_Rd(x_{139}) \quad \text{cnf}(\text{quest}_3, \text{negated_conjecture})$

$p_Wr(x_{139}) \quad \text{cnf}(\text{quest}_4, \text{negated_conjecture})$

$\text{level}(x_{139} + n_1) \neq \text{level}(x_{139}) + n_1 \quad \text{cnf}(\text{quest}_5, \text{negated_conjecture})$

HWV013-2.p Safelogic VHDL design verification obligation

include('Axioms/HWV004-0.ax')

$\neg p_pred_(\text{fwork_DOTfifo_DOTrtl_DOTreset_}(\text{t}_{206})) \quad \text{cnf}(\text{quest}_1, \text{negated_conjecture})$

$\neg p_pred_(\text{fwork_DOTfifo_DOTrtl_DOTrd_}(\text{t}_{206})) \quad \text{cnf}(\text{quest}_2, \text{negated_conjecture})$

$p_pred_(\text{fwork_DOTfifo_DOTrtl_DOTwr_}(\text{t}_{206})) \quad \text{cnf}(\text{quest}_3, \text{negated_conjecture})$

$\neg p_LES_EQU_(\text{fwork_DOTfifo_DOTrtl_DOTfifo_length_}, \text{fwork_DOTfifo_DOTrtl_DOTlevel_}(\text{t}_{206})) \quad \text{cnf}(\text{quest}_4, \text{negated_conjecture})$

$\text{fwork_DOTfifo_DOTrtl_DOTlevel_}(f_ADD_(\text{t}_{206}, n_1)) \neq f_ADD_(\text{fwork_DOTfifo_DOTrtl_DOTlevel_}(\text{t}_{206}), n_1) \quad \text{cnf}(\text{quest}_5, \text{negated_conjecture})$

HWV014-1.p Safelogic VHDL design verification obligation

include('Axioms/HWV003-0.ax')

$gt(\text{level}(x_{139}), n_0) \quad \text{cnf}(\text{quest}_1, \text{negated_conjecture})$

$p_Rd(x_{139}) \quad \text{cnf}(\text{quest}_2, \text{negated_conjecture})$

$\neg p_Wr(x_{139}) \quad \text{cnf}(\text{quest}_3, \text{negated_conjecture})$

$\neg p_Reset(x_{139}) \quad \text{cnf}(\text{quest}_4, \text{negated_conjecture})$

level($x_{139} + n_1$) \neq $-\text{level}(x_{139})$ cnf(quest₅, negated_conjecture)

HWV014-2.p Safelogic VHDL design verification obligation

include('Axioms/HWV004-0.ax')

\neg p_LES_EQU_(fwork_DOTfifo_DOTTrtl_DOTlevel_(t_{206}), n_0) cnf(quest₁, negated_conjecture)

\neg p_pred_(fwork_DOTfifo_DOTTrtl_DOTwr_(t_{206})) cnf(quest₂, negated_conjecture)

\neg p_pred_(fwork_DOTfifo_DOTTrtl_DOTreset_(t_{206})) cnf(quest₃, negated_conjecture)

p_pred_(fwork_DOTfifo_DOTTrtl_DOTrd_(t_{206})) cnf(quest₄, negated_conjecture)

fwork_DOTfifo_DOTTrtl_DOTlevel_(f_ADD_(t_{206} , n_1)) \neq f_SUB_(fwork_DOTfifo_DOTTrtl_DOTlevel_(t_{206}), n_1) cnf(quest₅, negated_conjecture)

HWV015-1.p Safelogic VHDL design verification obligation

include('Axioms/HWV003-0.ax')

gt(level(x_{139}), n_0) cnf(quest₁, negated_conjecture)

p_Rd(x_{139}) cnf(quest₂, negated_conjecture)

p_Wr(x_{139}) cnf(quest₃, negated_conjecture)

\neg p_Reset(x_{139}) cnf(quest₄, negated_conjecture)

level($x_{139} + n_1$) \neq level(x_{139}) cnf(quest₅, negated_conjecture)

HWV015-2.p Safelogic VHDL design verification obligation

include('Axioms/HWV004-0.ax')

\neg p_LES_EQU_(fwork_DOTfifo_DOTTrtl_DOTlevel_(t_{206}), n_0) cnf(quest₁, negated_conjecture)

p_pred_(fwork_DOTfifo_DOTTrtl_DOTwr_(t_{206})) cnf(quest₂, negated_conjecture)

\neg p_pred_(fwork_DOTfifo_DOTTrtl_DOTreset_(t_{206})) cnf(quest₃, negated_conjecture)

p_pred_(fwork_DOTfifo_DOTTrtl_DOTrd_(t_{206})) cnf(quest₄, negated_conjecture)

fwork_DOTfifo_DOTTrtl_DOTlevel_(f_ADD_(t_{206} , n_1)) \neq fwork_DOTfifo_DOTTrtl_DOTlevel_(t_{206}) cnf(quest₅, negated_conjecture)

HWV016-1.p Safelogic VHDL design verification obligation

include('Axioms/HWV003-0.ax')

\neg gt(n_0 , level(t_{139})) cnf(quest₁, negated_conjecture)

p_Wr(t_{139}) cnf(quest₂, negated_conjecture)

\neg p_Reset(t_{139}) cnf(quest₃, negated_conjecture)

p_Empty($t_{139} + n_1$) cnf(quest₄, negated_conjecture)

gt(fifo_length, n_0) cnf(quest₅, negated_conjecture)

HWV016-2.p Safelogic VHDL design verification obligation

include('Axioms/HWV004-0.ax')

p_LES_EQU_(n_0 , fwork_DOTfifo_DOTTrtl_DOTlevel_(t_{206})) cnf(quest₁, negated_conjecture)

\neg p_pred_(fwork_DOTfifo_DOTTrtl_DOTreset_(t_{206})) cnf(quest₂, negated_conjecture)

p_pred_(fwork_DOTfifo_DOTTrtl_DOTwr_(t_{206})) cnf(quest₃, negated_conjecture)

p_pred_(fwork_DOTfifo_DOTTrtl_DOTempty_(f_ADD_(t_{206} , n_1))) cnf(quest₄, negated_conjecture)

\neg p_LES_EQU_(fwork_DOTfifo_DOTTrtl_DOTfifo_length_, n_0) cnf(quest₅, negated_conjecture)

HWV017-1.p Safelogic VHDL design verification obligation

include('Axioms/HWV003-0.ax')

\neg gt(level(t_{139}), fifo_length) cnf(quest₁, negated_conjecture)

p_Rd(t_{139}) cnf(quest₂, negated_conjecture)

\neg p_Wr(t_{139}) cnf(quest₃, negated_conjecture)

\neg p_Reset(t_{139}) cnf(quest₄, negated_conjecture)

p_Full($t_{139} + n_1$) cnf(quest₅, negated_conjecture)

gt(fifo_length, n_0) cnf(quest₆, negated_conjecture)

HWV017-2.p Safelogic VHDL design verification obligation

include('Axioms/HWV004-0.ax')

p_LES_EQU_(fwork_DOTfifo_DOTTrtl_DOTlevel_(t_{206}), fwork_DOTfifo_DOTTrtl_DOTfifo_length_) cnf(quest₁, negated_conjecture)

\neg p_pred_(fwork_DOTfifo_DOTTrtl_DOTwr_(t_{206})) cnf(quest₂, negated_conjecture)

\neg p_pred_(fwork_DOTfifo_DOTTrtl_DOTreset_(t_{206})) cnf(quest₃, negated_conjecture)

p_pred_(fwork_DOTfifo_DOTTrtl_DOTrd_(t_{206})) cnf(quest₄, negated_conjecture)

p_pred_(fwork_DOTfifo_DOTTrtl_DOTfull_(f_ADD_(t_{206} , n_1))) cnf(quest₅, negated_conjecture)

\neg p_LES_EQU_(fwork_DOTfifo_DOTTrtl_DOTfifo_length_, n_0) cnf(quest₆, negated_conjecture)

HWV018-1.p Safelogic VHDL design verification obligation

include('Axioms/HWV003-0.ax')

\neg p_Rd(t_{139}) cnf(quest₁, negated_conjecture)

p_Wr(t_{139}) cnf(quest₂, negated_conjecture)

$p_Full(t_{139}) \quad cnf(quest_3, negated_conjecture)$
 $\neg p_Reset(t_{139}) \quad cnf(quest_4, negated_conjecture)$
 $p_Full(t_{139} + n_1) \Rightarrow \neg p_Wr_error(t_{139} + n_1) \quad cnf(quest_5, negated_conjecture)$

HWV018-2.p Safelogic VHDL design verification obligation

$include('Axioms/HWV004-0.ax')$
 $\neg p_pred_(\text{fwork_DOTfifo_DOTrtl_DOTrd}_-(t_{206})) \quad cnf(quest_1, negated_conjecture)$
 $p_pred_(\text{fwork_DOTfifo_DOTrtl_DOTfull}_-(t_{206})) \quad cnf(quest_2, negated_conjecture)$
 $\neg p_pred_(\text{fwork_DOTfifo_DOTrtl_DOTreset}_-(t_{206})) \quad cnf(quest_3, negated_conjecture)$
 $p_pred_(\text{fwork_DOTfifo_DOTrtl_DOTwr}_-(t_{206})) \quad cnf(quest_4, negated_conjecture)$
 $\neg p_pred_(\text{fwork_DOTfifo_DOTrtl_DOTfull}_-(f_ADD_-(t_{206}, n_1))) \quad cnf(quest_5, negated_conjecture)$

HWV018-3.p Safelogic VHDL design verification obligation

$include('Axioms/HWV004-0.ax')$
 $\neg p_pred_(\text{fwork_DOTfifo_DOTrtl_DOTrd}_-(t_{206})) \quad cnf(quest_1, negated_conjecture)$
 $p_pred_(\text{fwork_DOTfifo_DOTrtl_DOTfull}_-(t_{206})) \quad cnf(quest_2, negated_conjecture)$
 $\neg p_pred_(\text{fwork_DOTfifo_DOTrtl_DOTreset}_-(t_{206})) \quad cnf(quest_3, negated_conjecture)$
 $p_pred_(\text{fwork_DOTfifo_DOTrtl_DOTwr}_-(t_{206})) \quad cnf(quest_4, negated_conjecture)$
 $\neg p_pred_(\text{fwork_DOTfifo_DOTrtl_DOTwr_error}_-(f_ADD_-(t_{206}, n_1))) \quad cnf(quest_5, negated_conjecture)$

HWV019-1.p Safelogic VHDL design verification obligation

$include('Axioms/HWV003-0.ax')$
 $p_Wr_error(t_{139} + n_1) \quad cnf(quest_1, negated_conjecture)$
 $p_Wr(t_{139}) \quad cnf(quest_2, negated_conjecture)$
 $\neg p_Reset(t_{139}) \quad cnf(quest_3, negated_conjecture)$
 $gt(\text{fifo_length}, \text{level}(t_{139})) \text{ or } p_Rd(t_{139}) \quad cnf(quest_4, negated_conjecture)$

HWV019-2.p Safelogic VHDL design verification obligation

$include('Axioms/HWV004-0.ax')$
 $p_pred_(\text{fwork_DOTfifo_DOTrtl_DOTwr_error}_-(f_ADD_-(t_{206}, n_1))) \quad cnf(quest_1, negated_conjecture)$
 $\neg p_pred_(\text{fwork_DOTfifo_DOTrtl_DOTreset}_-(t_{206})) \quad cnf(quest_2, negated_conjecture)$
 $p_pred_(\text{fwork_DOTfifo_DOTrtl_DOTwr}_-(t_{206})) \quad cnf(quest_3, negated_conjecture)$
 $\neg p_LES_EQU_(\text{fwork_DOTfifo_DOTrtl_DOTfifo_length}_-, \text{fwork_DOTfifo_DOTrtl_DOTlevel}_-(t_{206})) \quad cnf(quest_4, negated_conjecture)$

HWV019-3.p Safelogic VHDL design verification obligation

$include('Axioms/HWV004-0.ax')$
 $p_pred_(\text{fwork_DOTfifo_DOTrtl_DOTwr_error}_-(f_ADD_-(t_{206}, n_1))) \quad cnf(quest_1, negated_conjecture)$
 $\neg p_pred_(\text{fwork_DOTfifo_DOTrtl_DOTreset}_-(t_{206})) \quad cnf(quest_2, negated_conjecture)$
 $p_pred_(\text{fwork_DOTfifo_DOTrtl_DOTwr}_-(t_{206})) \quad cnf(quest_3, negated_conjecture)$
 $p_pred_(\text{fwork_DOTfifo_DOTrtl_DOTrd}_-(t_{206})) \quad cnf(quest_4, negated_conjecture)$

HWV020-1.p Safelogic VHDL design verification obligation

$include('Axioms/HWV003-0.ax')$
 $p_Rd(t_{139}) \quad cnf(quest_1, negated_conjecture)$
 $p_Empty(t_{139}) \quad cnf(quest_2, negated_conjecture)$
 $\neg p_Wr(t_{139}) \quad cnf(quest_3, negated_conjecture)$
 $\neg p_Reset(t_{139}) \quad cnf(quest_4, negated_conjecture)$
 $p_Empty(t_{139} + n_1) \Rightarrow \neg p_Rd_error(t_{139} + n_1) \quad cnf(quest_5, negated_conjecture)$

HWV020-2.p Safelogic VHDL design verification obligation

$include('Axioms/HWV004-0.ax')$
 $p_pred_(\text{fwork_DOTfifo_DOTrtl_DOTrd}_-(t_{206})) \quad cnf(quest_1, negated_conjecture)$
 $\neg p_pred_(\text{fwork_DOTfifo_DOTrtl_DOTwr}_-(t_{206})) \quad cnf(quest_2, negated_conjecture)$
 $\neg p_pred_(\text{fwork_DOTfifo_DOTrtl_DOTreset}_-(t_{206})) \quad cnf(quest_3, negated_conjecture)$
 $p_pred_(\text{fwork_DOTfifo_DOTrtl_DOTempty}_-(t_{206})) \quad cnf(quest_4, negated_conjecture)$
 $\neg p_pred_(\text{fwork_DOTfifo_DOTrtl_DOTempty}_-(f_ADD_-(t_{206}, n_1))) \quad cnf(quest_5, negated_conjecture)$

HWV020-3.p Safelogic VHDL design verification obligation

$include('Axioms/HWV004-0.ax')$
 $p_pred_(\text{fwork_DOTfifo_DOTrtl_DOTrd}_-(t_{206})) \quad cnf(quest_1, negated_conjecture)$
 $\neg p_pred_(\text{fwork_DOTfifo_DOTrtl_DOTwr}_-(t_{206})) \quad cnf(quest_2, negated_conjecture)$
 $\neg p_pred_(\text{fwork_DOTfifo_DOTrtl_DOTreset}_-(t_{206})) \quad cnf(quest_3, negated_conjecture)$
 $p_pred_(\text{fwork_DOTfifo_DOTrtl_DOTempty}_-(t_{206})) \quad cnf(quest_4, negated_conjecture)$
 $\neg p_pred_(\text{fwork_DOTfifo_DOTrtl_DOTrd_error}_-(f_ADD_-(t_{206}, n_1))) \quad cnf(quest_5, negated_conjecture)$

HWV021-1.p Safelogic VHDL design verification obligation

```
include('Axioms/HWV003-0.ax')
p_Rd_error(t139 + n1)    cnf(quest1, negated_conjecture)
p_Rd(t139)    cnf(quest2, negated_conjecture)
¬ p_Reset(t139)    cnf(quest3, negated_conjecture)
¬ p_Empty(t139)    cnf(quest4, negated_conjecture)
```

HWV021-2.p Safelogic VHDL design verification obligation

```
include('Axioms/HWV004-0.ax')
p_pred_(fwork_DOTfifo_DOTTrtl_DOTTrd_error_(f_ADD_(t206, n1)))    cnf(quest1, negated_conjecture)
¬ p_pred_(fwork_DOTfifo_DOTTrtl_DOTReset_(t206))    cnf(quest2, negated_conjecture)
p_pred_(fwork_DOTfifo_DOTTrtl_DOTTrd_(t206))    cnf(quest3, negated_conjecture)
¬ p_pred_(fwork_DOTfifo_DOTTrtl_DOTEmpty_(t206))    cnf(quest4, negated_conjecture)
```

HWV022-1.p Safelogic VHDL design verification obligation

```
include('Axioms/HWV003-0.ax')
level(t139) + n1 = fifo_length    cnf(quest1, negated_conjecture)
¬ p_Rd(t139)    cnf(quest2, negated_conjecture)
p_Wr(t139)    cnf(quest3, negated_conjecture)
¬ p_Reset(t139)    cnf(quest4, negated_conjecture)
level(t139 + n1) ≠ fifo_length    cnf(quest5, negated_conjecture)
```

HWV022-2.p Safelogic VHDL design verification obligation

```
include('Axioms/HWV004-0.ax')
f_ADD_(fwork_DOTfifo_DOTTrtl_DOTlevel_(t206), n1) = fwork_DOTfifo_DOTTrtl_DOTfifo_length_    cnf(quest1, negated_conj...
p_pred_(fwork_DOTfifo_DOTTrtl_DOTWr_(t206))    cnf(quest2, negated_conjecture)
¬ p_pred_(fwork_DOTfifo_DOTTrtl_DOTReset_(t206))    cnf(quest3, negated_conjecture)
¬ p_pred_(fwork_DOTfifo_DOTTrtl_DOTTrd_(t206))    cnf(quest4, negated_conjecture)
fwork_DOTfifo_DOTTrtl_DOTlevel_(f_ADD_(t206, n1)) ≠ fwork_DOTfifo_DOTTrtl_DOTfifo_length_    cnf(quest5, negated_conj...
```

HWV023-1.p Safelogic VHDL design verification obligation

```
include('Axioms/HWV003-0.ax')
level(t139) = n1    cnf(quest1, negated_conjecture)
¬ p_Wr(t139)    cnf(quest2, negated_conjecture)
p_Rd(t139)    cnf(quest3, negated_conjecture)
¬ p_Reset(t139)    cnf(quest4, negated_conjecture)
¬ p_Empty(t139 + n1)    cnf(quest5, negated_conjecture)
```

HWV023-2.p Safelogic VHDL design verification obligation

```
include('Axioms/HWV004-0.ax')
fwork_DOTfifo_DOTTrtl_DOTlevel_(t206) = n1    cnf(quest1, negated_conjecture)
p_pred_(fwork_DOTfifo_DOTTrtl_DOTTrd_(t206))    cnf(quest2, negated_conjecture)
¬ p_pred_(fwork_DOTfifo_DOTTrtl_DOTReset_(t206))    cnf(quest3, negated_conjecture)
¬ p_pred_(fwork_DOTfifo_DOTTrtl_DOTWr_(t206))    cnf(quest4, negated_conjecture)
¬ p_pred_(fwork_DOTfifo_DOTTrtl_DOTEmpty_(f_ADD_(t206, n1)))    cnf(quest5, negated_conjecture)
```

HWV024-1.p Safelogic VHDL design verification obligation

```
include('Axioms/HWV003-0.ax')
¬ p_Rd(x140)    cnf(quest1, negated_conjecture)
¬ p_Reset(x140)    cnf(quest2, negated_conjecture)
p_Data_out(x139, x140) ⇒ ¬ p_Data_out(x139, x140 + n1)    cnf(quest3, negated_conjecture)
p_Data_out(x139, x140) or p_Data_out(x139, x140 + n1)    cnf(quest4, negated_conjecture)
```

HWV024-2.p Safelogic VHDL design verification obligation

```
include('Axioms/HWV004-0.ax')
¬ p_pred_(fwork_DOTfifo_DOTTrtl_DOTTrd_(t206))    cnf(quest1, negated_conjecture)
¬ p_pred_(fwork_DOTfifo_DOTTrtl_DOTReset_(t206))    cnf(quest2, negated_conjecture)
p_LES_EQU_(n0, x207)    cnf(quest3, negated_conjecture)
p_LES_EQU_(x207, f.SUB_(fwork_DOTfifo_DOTTrtl_DOTfifo_width_, n1))    cnf(quest4, negated_conjecture)
f_index_(fwork_DOTfifo_DOTTrtl_DOTdata_out_(f_ADD_(t206, n1)), f.SUB_(f.SUB_(fwork_DOTfifo_DOTTrtl_DOTfifo_width_, n1), x207))
f_index_(fwork_DOTfifo_DOTTrtl_DOTdata_out_(t206), f.SUB_(f.SUB_(fwork_DOTfifo_DOTTrtl_DOTfifo_width_, n1), x207))
```

HWV025-1.p Safelogic VHDL design verification obligation

```
include('Axioms/HWV003-0.ax')
```

```

¬ p_Rd( $t_{139}$ )      cnf(quest1, negated_conjecture)
¬ p_Reset( $t_{139}$ )    cnf(quest2, negated_conjecture)
p_Rd_error( $t_{139}$ ) ⇒ ¬ p_Rd_error( $t_{139} + n_1$ )  cnf(quest3, negated_conjecture)
p_Rd_error( $t_{139}$ ) or p_Rd_error( $t_{139} + n_1$ )  cnf(quest4, negated_conjecture)

```

HWV025-2.p Safelogic VHDL design verification obligation

```

include('Axioms/HWV004-0.ax')
¬ p__pred_(fwork_DOTfifo_DOTrtl_DOTrd_( $t_{206}$ ))  cnf(quest1, negated_conjecture)
¬ p__pred_(fwork_DOTfifo_DOTrtl_DOTreset_( $t_{206}$ ))  cnf(quest2, negated_conjecture)
¬ p__pred_(fwork_DOTfifo_DOTrtl_DOTrd__error_(f_ADD_( $t_{206}, n_1$ )))  cnf(quest3, negated_conjecture)
p__pred_(fwork_DOTfifo_DOTrtl_DOTrd__error_( $t_{206}$ ))  cnf(quest4, negated_conjecture)

```

HWV025-3.p Safelogic VHDL design verification obligation

```

include('Axioms/HWV004-0.ax')
¬ p__pred_(fwork_DOTfifo_DOTrtl_DOTrd_( $t_{206}$ ))  cnf(quest1, negated_conjecture)
¬ p__pred_(fwork_DOTfifo_DOTrtl_DOTreset_( $t_{206}$ ))  cnf(quest2, negated_conjecture)
p__pred_(fwork_DOTfifo_DOTrtl_DOTrd__error_(f_ADD_( $t_{206}, n_1$ )))  cnf(quest3, negated_conjecture)
¬ p__pred_(fwork_DOTfifo_DOTrtl_DOTrd__error_( $t_{206}$ ))  cnf(quest4, negated_conjecture)

```

HWV026-1.p Safelogic VHDL design verification obligation

```

include('Axioms/HWV003-0.ax')
¬ p_Wr( $t_{139}$ )      cnf(quest1, negated_conjecture)
¬ p_Reset( $t_{139}$ )    cnf(quest2, negated_conjecture)
p_Wr_error( $t_{139}$ ) ⇒ ¬ p_Wr_error( $t_{139} + n_1$ )  cnf(quest3, negated_conjecture)
p_Wr_error( $t_{139}$ ) or p_Wr_error( $t_{139} + n_1$ )  cnf(quest4, negated_conjecture)

```

HWV026-2.p Safelogic VHDL design verification obligation

```

include('Axioms/HWV004-0.ax')
¬ p__pred_(fwork_DOTfifo_DOTrtl_DOTwr_( $t_{206}$ ))  cnf(quest1, negated_conjecture)
¬ p__pred_(fwork_DOTfifo_DOTrtl_DOTreset_( $t_{206}$ ))  cnf(quest2, negated_conjecture)
¬ p__pred_(fwork_DOTfifo_DOTrtl_DOTwr__error_(f_ADD_( $t_{206}, n_1$ )))  cnf(quest3, negated_conjecture)
p__pred_(fwork_DOTfifo_DOTrtl_DOTwr__error_( $t_{206}$ ))  cnf(quest4, negated_conjecture)

```

HWV026-3.p Safelogic VHDL design verification obligation

```

include('Axioms/HWV004-0.ax')
¬ p__pred_(fwork_DOTfifo_DOTrtl_DOTwr_( $t_{206}$ ))  cnf(quest1, negated_conjecture)
¬ p__pred_(fwork_DOTfifo_DOTrtl_DOTreset_( $t_{206}$ ))  cnf(quest2, negated_conjecture)
p__pred_(fwork_DOTfifo_DOTrtl_DOTwr__error_(f_ADD_( $t_{206}, n_1$ )))  cnf(quest3, negated_conjecture)
¬ p__pred_(fwork_DOTfifo_DOTrtl_DOTwr__error_( $t_{206}$ ))  cnf(quest4, negated_conjecture)

```

HWV027-1.p Safelogic VHDL design verification obligation

```

include('Axioms/HWV003-0.ax')
¬ p_Wr( $t_{139}$ )      cnf(quest1, negated_conjecture)
¬ p_Rd( $t_{139}$ )      cnf(quest2, negated_conjecture)
¬ p_Reset( $t_{139}$ )    cnf(quest3, negated_conjecture)
level( $t_{139}$ ) ≠ level( $t_{139} + n_1$ )  cnf(quest4, negated_conjecture)

```

HWV027-2.p Safelogic VHDL design verification obligation

```

include('Axioms/HWV004-0.ax')
¬ p__pred_(fwork_DOTfifo_DOTrtl_DOTwr_( $t_{206}$ ))  cnf(quest1, negated_conjecture)
¬ p__pred_(fwork_DOTfifo_DOTrtl_DOTreset_( $t_{206}$ ))  cnf(quest2, negated_conjecture)
¬ p__pred_(fwork_DOTfifo_DOTrtl_DOTrd_( $t_{206}$ ))  cnf(quest3, negated_conjecture)
fwork_DOTfifo_DOTrtl_DOTlevel_( $t_{206}$ ) ≠ fwork_DOTfifo_DOTrtl_DOTlevel_(f_ADD_( $t_{206}, n_1$ ))  cnf(quest4, negated_conj)

```

HWV028-1.p Safelogic VHDL design verification obligation

```

include('Axioms/HWV003-0.ax')
p_Reset( $t_{139}$ )      cnf(quest1, negated_conjecture)
gt(level( $t_{139} + n_1$ ), fifo_length)  cnf(quest2, negated_conjecture)
gt(fifo_length,  $n_0$ )  cnf(quest3, negated_conjecture)

```

HWV028-2.p Safelogic VHDL design verification obligation

```

include('Axioms/HWV004-0.ax')
p__pred_(fwork_DOTfifo_DOTrtl_DOTreset_( $t_{206}$ ))  cnf(quest1, negated_conjecture)
¬ p_LES_EQU_(fwork_DOTfifo_DOTrtl_DOTlevel_(f_ADD_( $t_{206}, n_1$ )), fwork_DOTfifo_DOTrtl_DOTfifo_length_)  cnf(quest2, negated_conj)
¬ p_LES_EQU_(fwork_DOTfifo_DOTrtl_DOTfifo_length_,  $n_0$ )  cnf(quest3, negated_conjecture)

```

HWV029-1.p Safelogic VHDL design verification obligation

```
include('Axioms/HWV003-0.ax')
¬ gt(level(x139), fifo_length)    cnf(quest1, negated_conjecture)
gt(level(x139 + n1), fifo_length)  cnf(quest2, negated_conjecture)
gt(fifo_length, n0)    cnf(quest3, negated_conjecture)
```

HWV029-2.p Safelogic VHDL design verification obligation

```
include('Axioms/HWV004-0.ax')
p_LES_EQU_(fwork_DOTfifo_DOTTrtl_DOTlevel_(t206), fwork_DOTfifo_DOTTrtl_DOTfifo_length_)    cnf(quest1, negated_conj
¬ p_LES_EQU_(fwork_DOTfifo_DOTTrtl_DOTlevel_(f_ADD_(t206, n1)), fwork_DOTfifo_DOTTrtl_DOTfifo_length_)    cnf(quest
¬ p_LES_EQU_(fwork_DOTfifo_DOTTrtl_DOTfifo_length_, n0)    cnf(quest3, negated_conjecture)
```

HWV030-1.p Safelogic VHDL design verification obligation

```
include('Axioms/HWV003-0.ax')
p_Reset(t139)    cnf(quest1, negated_conjecture)
¬ gt(fifo_length, wr_level(t139 + n1))    cnf(quest2, negated_conjecture)
gt(fifo_length, n0)    cnf(quest3, negated_conjecture)
```

HWV030-2.p Safelogic VHDL design verification obligation

```
include('Axioms/HWV004-0.ax')
p_pred_(fwork_DOTfifo_DOTTrtl_DOTTreset_(t206))    cnf(quest1, negated_conjecture)
p_LES_EQU_(fwork_DOTfifo_DOTTrtl_DOTfifo_length_, fwork_DOTfifo_DOTTrtl_DOTwr_level_(f_ADD_(t206, n1)))    cnf(qu
¬ p_LES_EQU_(fwork_DOTfifo_DOTTrtl_DOTfifo_length_, n0)    cnf(quest3, negated_conjecture)
```

HWV031-1.p Safelogic VHDL design verification obligation

```
include('Axioms/HWV003-0.ax')
¬ gt(wr_level(x139) + n1, fifo_length)    cnf(quest1, negated_conjecture)
gt(wr_level(x139 + n1) + n1, fifo_length)    cnf(quest2, negated_conjecture)
gt(fifo_length, n0)    cnf(quest3, negated_conjecture)
```

HWV031-2.p Safelogic VHDL design verification obligation

```
include('Axioms/HWV004-0.ax')
p_LES_EQU_(f_ADD_(fwork_DOTfifo_DOTTrtl_DOTwr_level_(t206), n1), fwork_DOTfifo_DOTTrtl_DOTfifo_length_)    cnf(qu
¬ p_LES_EQU_(f_ADD_(fwork_DOTfifo_DOTTrtl_DOTwr_level_(f_ADD_(t206, n1)), n1), fwork_DOTfifo_DOTTrtl_DOTfifo_length_)
¬ p_LES_EQU_(fwork_DOTfifo_DOTTrtl_DOTfifo_length_, n0)    cnf(quest3, negated_conjecture)
```

HWV032-1.p Safelogic VHDL design verification obligation

```
include('Axioms/HWV003-0.ax')
p_Reset(t139)    cnf(quest1, negated_conjecture)
¬ gt(fifo_length, rd_level(t139 + n1))    cnf(quest2, negated_conjecture)
gt(fifo_length, n0)    cnf(quest3, negated_conjecture)
```

HWV032-2.p Safelogic VHDL design verification obligation

```
include('Axioms/HWV004-0.ax')
p_pred_(fwork_DOTfifo_DOTTrtl_DOTTreset_(t206))    cnf(quest1, negated_conjecture)
p_LES_EQU_(fwork_DOTfifo_DOTTrtl_DOTfifo_length_, fwork_DOTfifo_DOTTrtl_DOTrd_level_(f_ADD_(t206, n1)))    cnf(que
¬ p_LES_EQU_(fwork_DOTfifo_DOTTrtl_DOTfifo_length_, n0)    cnf(quest3, negated_conjecture)
```

HWV033-1.p Safelogic VHDL design verification obligation

```
include('Axioms/HWV003-0.ax')
¬ gt(rd_level(t139), -fifo_length)    cnf(quest1, negated_conjecture)
gt(rd_level(t139 + n1), -fifo_length)    cnf(quest2, negated_conjecture)
gt(fifo_length, n0)    cnf(quest3, negated_conjecture)
```

HWV033-2.p Safelogic VHDL design verification obligation

```
include('Axioms/HWV004-0.ax')
p_LES_EQU_(fwork_DOTfifo_DOTTrtl_DOTrd_level_(t206), f_SUB_(fwork_DOTfifo_DOTTrtl_DOTfifo_length_, n1))    cnf(que
¬ p_LES_EQU_(fwork_DOTfifo_DOTTrtl_DOTrd_level_(f_ADD_(t206, n1)), f_SUB_(fwork_DOTfifo_DOTTrtl_DOTfifo_length_, n
¬ p_LES_EQU_(fwork_DOTfifo_DOTTrtl_DOTfifo_length_, n0)    cnf(quest3, negated_conjecture)
```

HWV034-1.p Connections, faults, and gates.

```
include('Axioms/HWV001-0.ax')
```

HWV034-2.p Connections, faults, and gates.

```
include('Axioms/HWV002-0.ax')
```

HWV035-1.p Half-adder.

```
include('Axioms/HWV001-0.ax')
include('Axioms/HWV001-1.ax')
```

HWV035-2.p Half-adder.

```
include('Axioms/HWV002-0.ax')
include('Axioms/HWV002-1.ax')
```

HWV036-1.p Full-adder.

```
include('Axioms/HWV001-0.ax')
include('Axioms/HWV001-1.ax')
include('Axioms/HWV001-2.ax')
```

HWV036-2.p Full-adder.

```
include('Axioms/HWV002-0.ax')
include('Axioms/HWV002-1.ax')
include('Axioms/HWV002-2.ax')
```

HWV037-1.p Axioms from a VHDL design description

```
include('Axioms/HWV003-0.ax')
```

HWV038-1.p Axioms from a VHDL design description

```
include('Axioms/HWV004-0.ax')
```

HWV052-1.001.001.p Faulty channel 1 1

The problem of sending N bits over a faulty channel that can mutilate any one bit. We can use K extra bits to help us do this. Satisfiable means that it is possible, unsatisfiable means that it is not possible.

```
 $x = o$  or  $x = i$     cnf(bit_domain, axiom)
 $x^{-1} \neq x$       cnf(bit_inverse, axiom)
unpack1( $x_1$ , pack1( $x_1$ )) =  $x_1$     cnf(unpack1, axiom)
unpack1( $x_1^{-1}$ , pack1( $x_1$ )) =  $x_1$     cnf(unpack101, axiom)
unpack1( $x_1$ , pack1( $x_1$ )-1) =  $x_1$     cnf(unpack102, axiom)
```

HWV052-1.001.002.p Faulty channel 1 2

The problem of sending N bits over a faulty channel that can mutilate any one bit. We can use K extra bits to help us do this. Satisfiable means that it is possible, unsatisfiable means that it is not possible.

```
 $x = o$  or  $x = i$     cnf(bit_domain, axiom)
 $x^{-1} \neq x$       cnf(bit_inverse, axiom)
unpack1( $x_1$ , pack1( $x_1$ ), pack2( $x_1$ )) =  $x_1$     cnf(unpack1, axiom)
unpack1( $x_1^{-1}$ , pack1( $x_1$ ), pack2( $x_1$ )) =  $x_1$     cnf(unpack101, axiom)
unpack1( $x_1$ , pack1( $x_1$ )-1, pack2( $x_1$ )) =  $x_1$     cnf(unpack102, axiom)
unpack1( $x_1$ , pack1( $x_1$ ), pack2( $x_1$ )-1) =  $x_1$     cnf(unpack103, axiom)
```

HWV052-1.002.001.p Faulty channel 2 1

The problem of sending N bits over a faulty channel that can mutilate any one bit. We can use K extra bits to help us do this. Satisfiable means that it is possible, unsatisfiable means that it is not possible.

```
 $x = o$  or  $x = i$     cnf(bit_domain, axiom)
 $x^{-1} \neq x$       cnf(bit_inverse, axiom)
unpack1( $x_1$ ,  $x_2$ , pack1( $x_1$ ,  $x_2$ )) =  $x_1$     cnf(unpack1, axiom)
unpack1( $x_1^{-1}$ ,  $x_2$ , pack1( $x_1$ ,  $x_2$ )) =  $x_1$     cnf(unpack101, axiom)
unpack1( $x_1$ ,  $x_2^{-1}$ , pack1( $x_1$ ,  $x_2$ )) =  $x_1$     cnf(unpack102, axiom)
unpack1( $x_1$ ,  $x_2$ , pack1( $x_1$ ,  $x_2$ )-1) =  $x_1$     cnf(unpack103, axiom)
unpack2( $x_1$ ,  $x_2$ , pack1( $x_1$ ,  $x_2$ )) =  $x_2$     cnf(unpack2, axiom)
unpack2( $x_1^{-1}$ ,  $x_2$ , pack1( $x_1$ ,  $x_2$ )) =  $x_2$     cnf(unpack204, axiom)
unpack2( $x_1$ ,  $x_2^{-1}$ , pack1( $x_1$ ,  $x_2$ )) =  $x_2$     cnf(unpack205, axiom)
unpack2( $x_1$ ,  $x_2$ , pack1( $x_1$ ,  $x_2$ )-1) =  $x_2$     cnf(unpack206, axiom)
```

HWV052-1.002.002.p Faulty channel 2 2

The problem of sending N bits over a faulty channel that can mutilate any one bit. We can use K extra bits to help us do this. Satisfiable means that it is possible, unsatisfiable means that it is not possible.

```
 $x = o$  or  $x = i$     cnf(bit_domain, axiom)
 $x^{-1} \neq x$       cnf(bit_inverse, axiom)
unpack1( $x_1$ ,  $x_2$ , pack1( $x_1$ ,  $x_2$ ), pack2( $x_1$ ,  $x_2$ )) =  $x_1$     cnf(unpack1, axiom)
unpack1( $x_1^{-1}$ ,  $x_2$ , pack1( $x_1$ ,  $x_2$ ), pack2( $x_1$ ,  $x_2$ )) =  $x_1$     cnf(unpack101, axiom)
unpack1( $x_1$ ,  $x_2^{-1}$ , pack1( $x_1$ ,  $x_2$ ), pack2( $x_1$ ,  $x_2$ )) =  $x_1$     cnf(unpack102, axiom)
```

